eFPGA Core® IP
The embedded Field Programmable Gate Array IP

Menta® eFPGA Core® IP is a high-density embedded programmable logic architecture IP designed to be used in SoC, ASIC or as standalone component, becoming a FPGA. The eFPGA Core IP provides design flexibility and reduces time-to-market by enabling lifetime reprogrammability. The technology allows logic functionality to be changed after manufacturing, reduces the number of chip redesigns and amortizes chip development costs over several design derivatives. This is the ideal solution for semiconductor companies wanting to add configurability to their end products.

The Menta eFPGA Core IP integrates smoothly into any standard ASIC methodology and design flow. Available as a fully synthesizable core for design portability and flexibility with the Menta Origami Designer™ environment, or as hard macro cell for high performance, low power and small die size solution, the eFPGA Core IP can targeted to any silicon foundry (IDMs and pure-plays). Application mapping, configuration and place and route design steps are performed by Menta Origami Programmer™ tool suite, which is compatible with most third-party design entry, verification and test tools.
Key Benefits
- Designed specifically for SoC, ASIC or SiP integration
- Highly customizable and scalable architecture
- Manufacturing DFT with full testability
- SPI/JTAG configuration system
- Versatile application synthesis, mapping, place and route tools

Architecture
The main building blocks of the eFPGA Core IP architecture is the eLB (embedded Logic Block). It is a configurable logic block interconnected as an array using programmable routing resources. To support high-speed arithmetic functions, a hardwired carry chain is included that connects directly eLB between them. Additional specific blocks can be inserted inside the array to customize the architecture in order to increase performances for application-oriented design. This includes dedicated arithmetic operator or custom block (eCB), such as multiplier, adder, shifter, etc. or customer block, or memory (eMB).

The eFPGA Core IP is scalable and highly customizable. Configuration parameters include: Look-Up Table (LUT) size, cluster size, hard macro block, interconnect bus width, etc. and number of IO.

The aspect ratio and shape of the core can be tailored to obtain the optimum design fit on the SoC device.

Configuration
A configuration interface provides the means to configure the eFPGA Core IP. It supports SPI modes or can alternatively be configured through the JTAG interface.

Manufacturing Test
The eFPGA Core IP grant a full DFT compatibility with all the most ASIC test solutions and an easy integration. Different test patterns are available to achieve very high fault coverage.

Programming tools
eFPGA Core IP is enabled and configured using the Menta Origami Programmer™ tool suite. Menta Origami Programmer encapsulates all the necessary design steps of a classical FPGA design flow, from RTL (VHDL, SystemVerilog or Verilog) to the programming bitstream.

Results
The eFPGA Core IP has been fully evaluated in 130 nm, 65 nm, 28 nm processes and ongoing in 14 nm.

The below figure shows an example of an eLB-based eFPGA Core IP used as standalone FPGA component.

Availability
Menta eFPGA Core IP is available now, as physical IP, on selected processes generated by Menta Origami Generator™. The hard macro of the eFPGA Core IP, an ideal drop-in solution for rapid time to market can be adapted to other process and customer requirements by leveraging Menta’s Design Services.

For more information about Menta products or support services, visit us on the web at: www.menta-efpga.com or contact sales@menta-efpga.com